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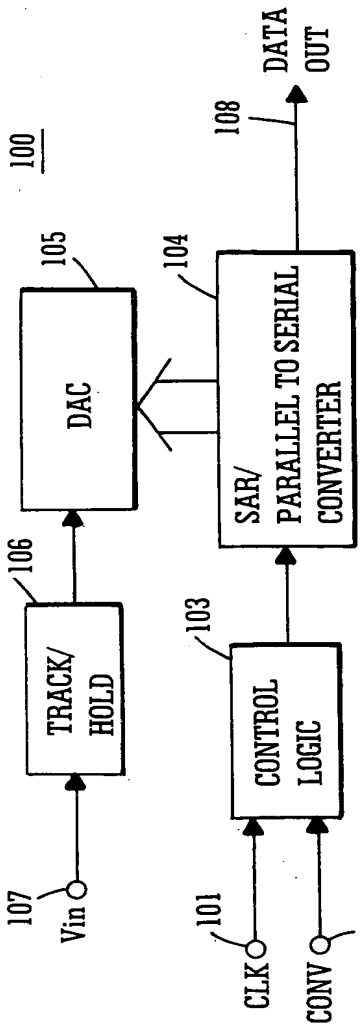
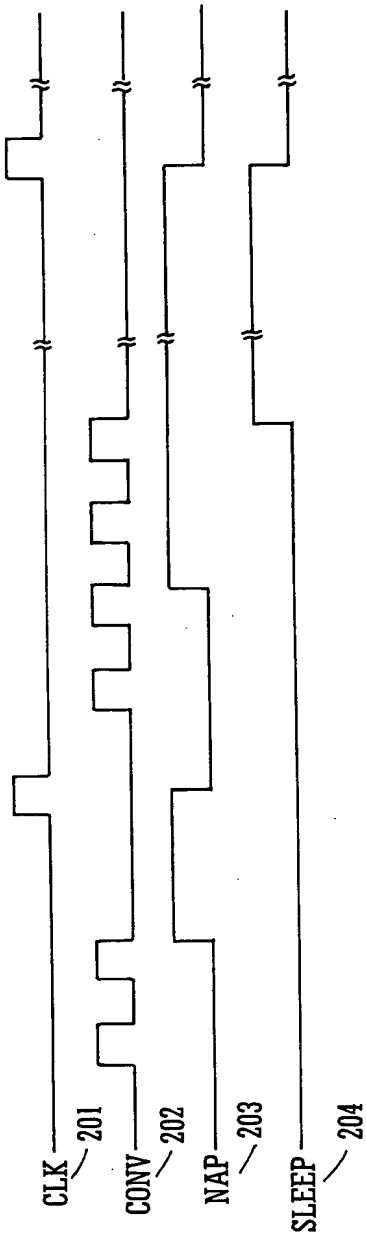


PRIOR ART
FIG. 1



PRIOR ART
FIG. 2

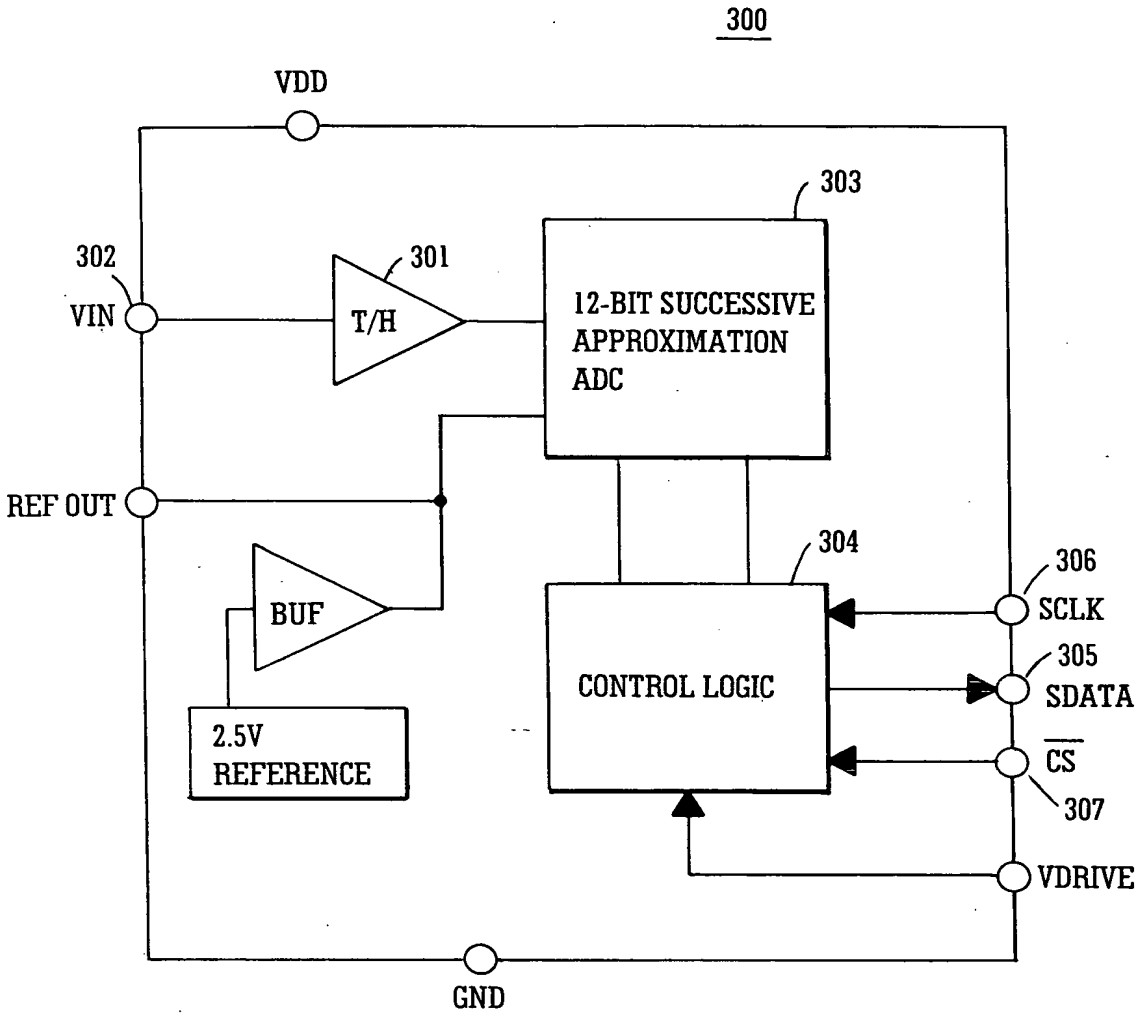

300
VDD
303
302
301
VIN
T/H
12-BIT SUCCESSIVE
APPROXIMATION
ADC
REF OUT
304
306
BUF
SCLK
305
CONTROL LOGIC
SDATA
2.5V
REFERENCE
CS
307
VDRIVE
GND

FIG. 3

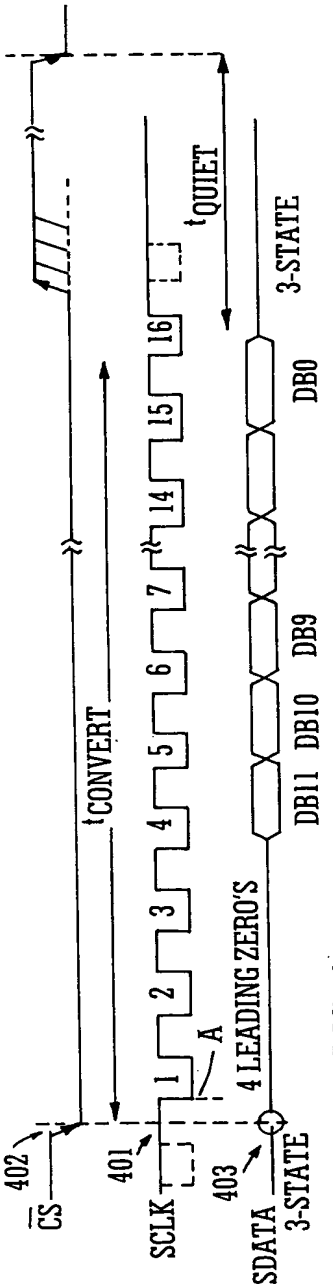


FIG. 4

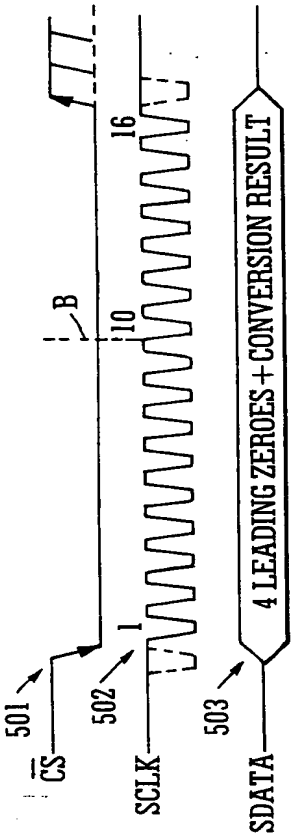


FIG. 5

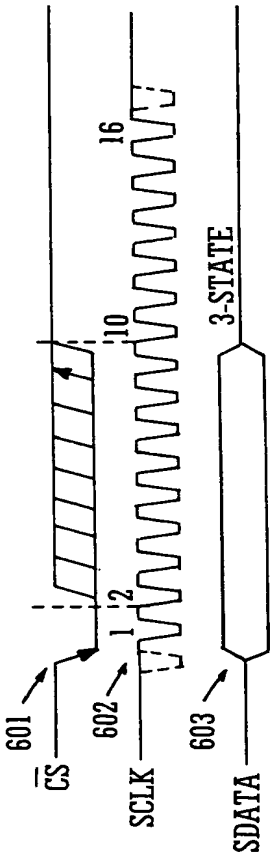


FIG. 6

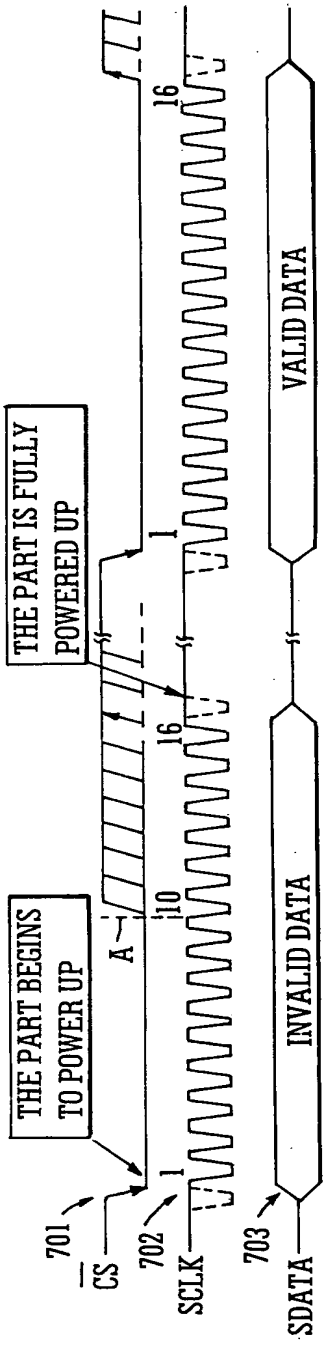


FIG. 7

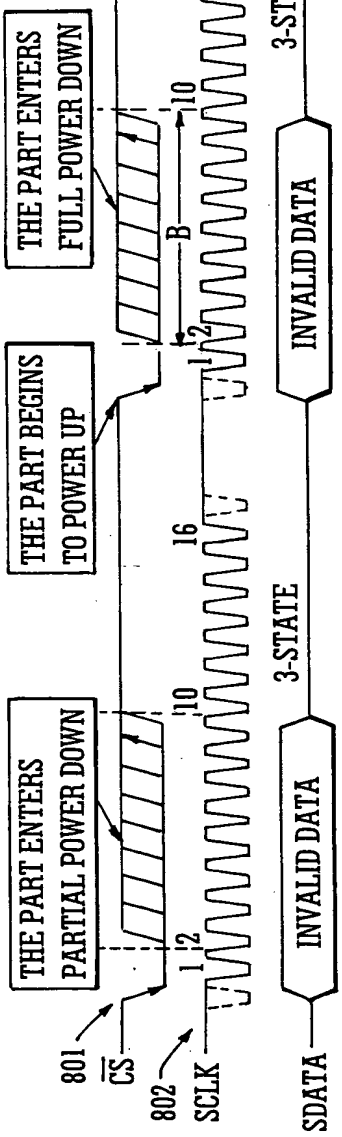


FIG. 8

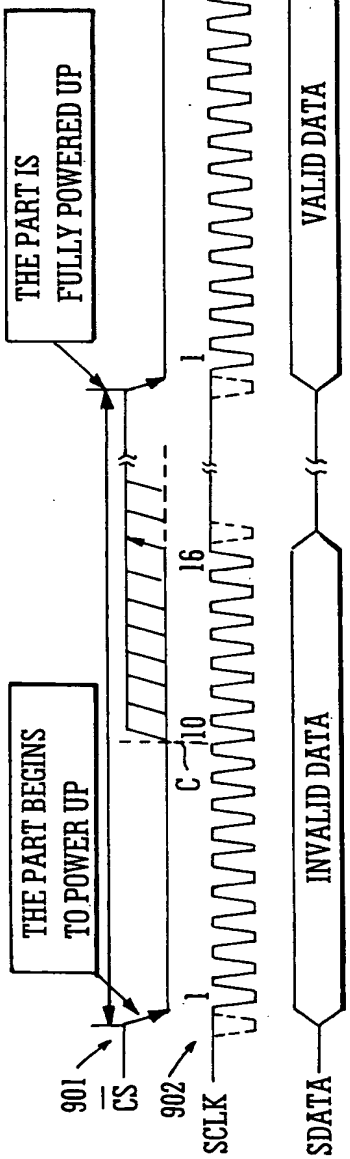


FIG. 9

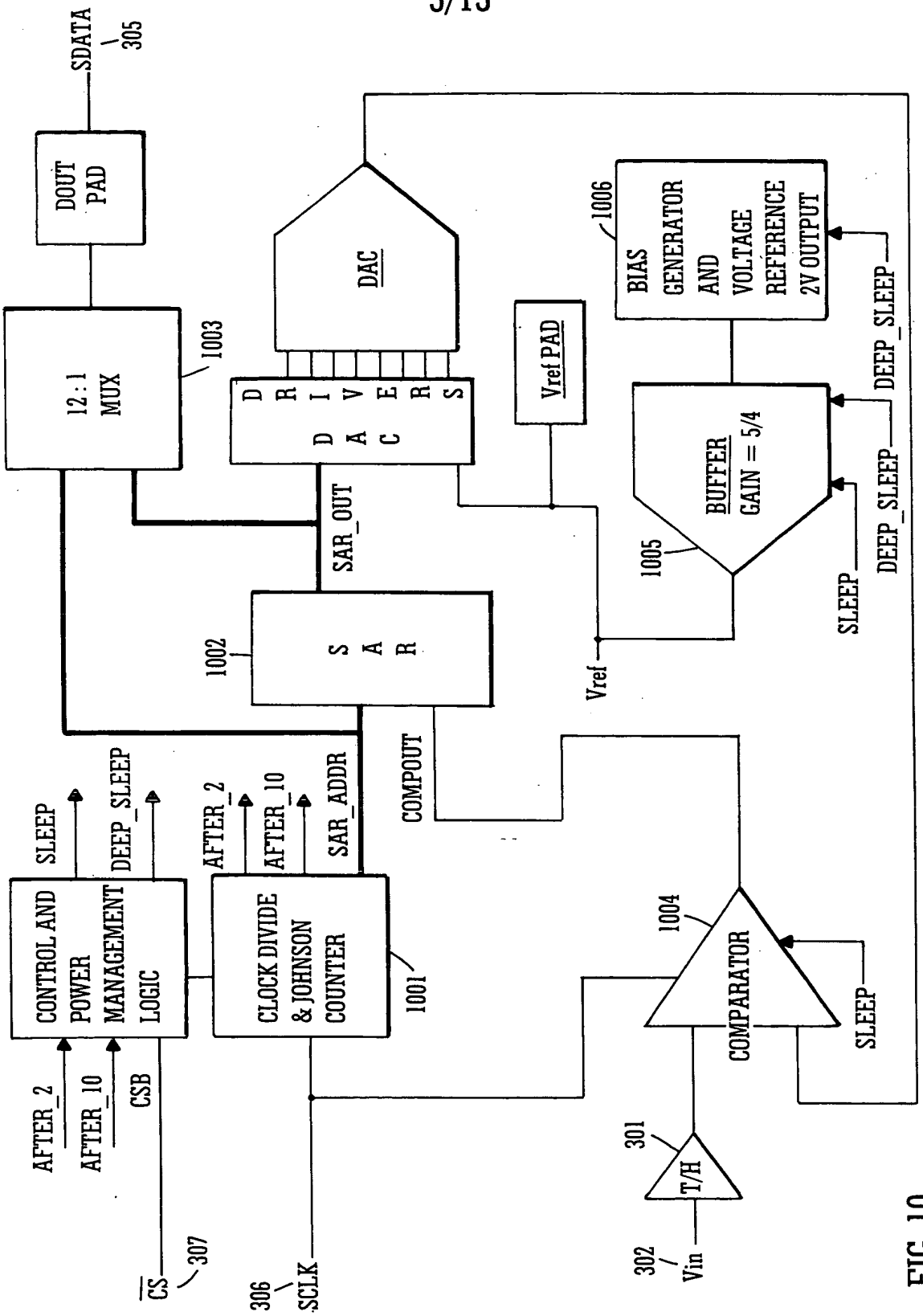

SDATA
305
DOUT PAD
12:1 MUX
1003
DAC
DRIVER
Vref PAD
1006
BIAS GENERATOR AND VOLTAGE REFERENCE 2V OUTPUT
DEEP_SLEEP
BUFFER GAIN = 5/4
1005
SLEEP
DEEP_SLEEP
SAR_OUT
1002
SAR
Vref
COMPOUT
SLEEP
DEEP_SLEEP
AFTER_2
AFTER_10
SAR_ADDR
CONTROL AND POWER MANAGEMENT LOGIC
CLOCK DIVIDE & JOHNSON COUNTER
1001
1004
COMPARATOR
SLEEP
AFTER_2
AFTER_10
CSB
301
T/H
302
Vin
CS
307
306
SCLK

FIG. 10

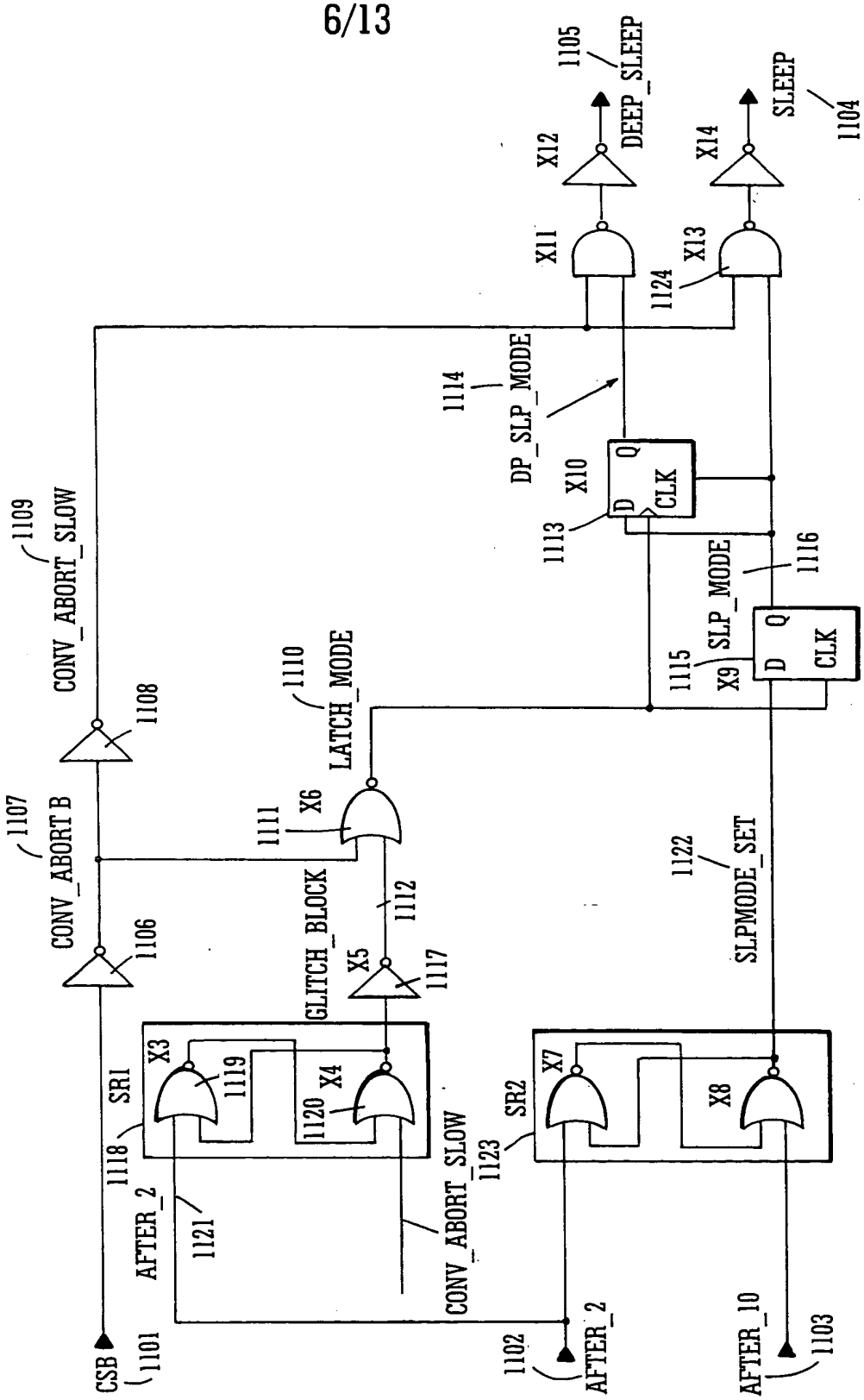

CSB
1101
AFTER_2
1121
SR1
1118
X3
1119
X4
1120
GLITCH_BLOCK
X5
1117
1112
CONV_ABORT_SLOW
1123
SR2
X7
X8
SLPMODE_SET
1122
AFTER_10
1103
AFTER_2
1102
CONV_ABORT B
1107
1106
CONV_ABORT_SLOW
1109
1108
LATCH_MODE
1110
X6
1111
DP_SLP_MODE
1114
X10
D
Q
CLK
1113
SLP_MODE
1116
X9
1115
X11
X12
DEEP_SLEEP
1105
X13
X14
SLEEP
1104
1124

FIG. 11

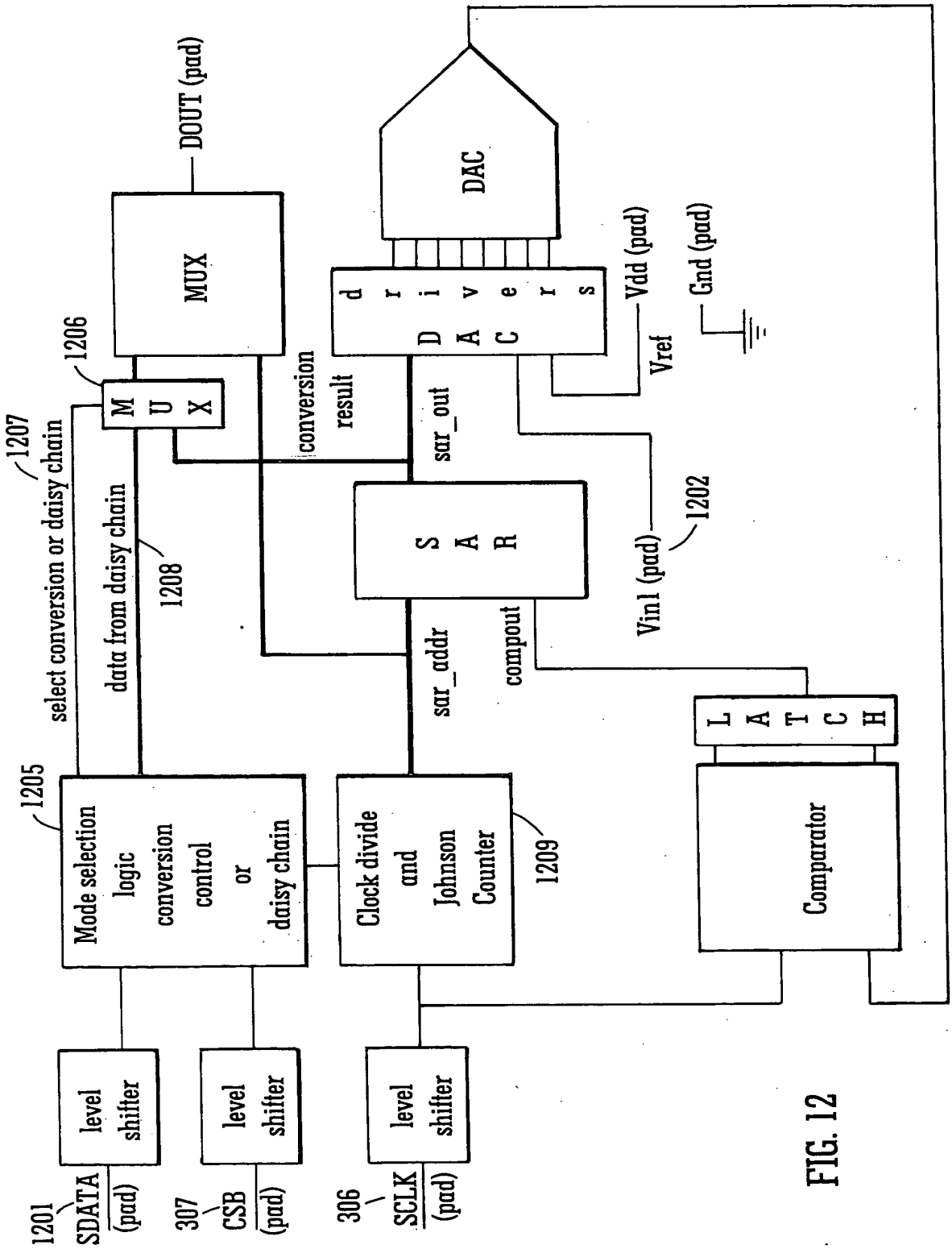

DOUT (pad)
MUX
DAC
1206
M U X
d r i v e r s
D A C
Vdd (pad)
Gnd (pad)
Vref
1207
select conversion or daisy chain
data from daisy chain
1208
conversion result
sar_out
S A R
1202
Vin1 (pad)
sar_addr
compout
L A T C H
Comparator
1205
Mode selection logic conversion control or daisy chain
Clock divide and Johnson Counter
1209
level shifter
level shifter
level shifter
1201
SDATA (pad)
307
CSB (pad)
306
SCLK (pad)

FIG. 12

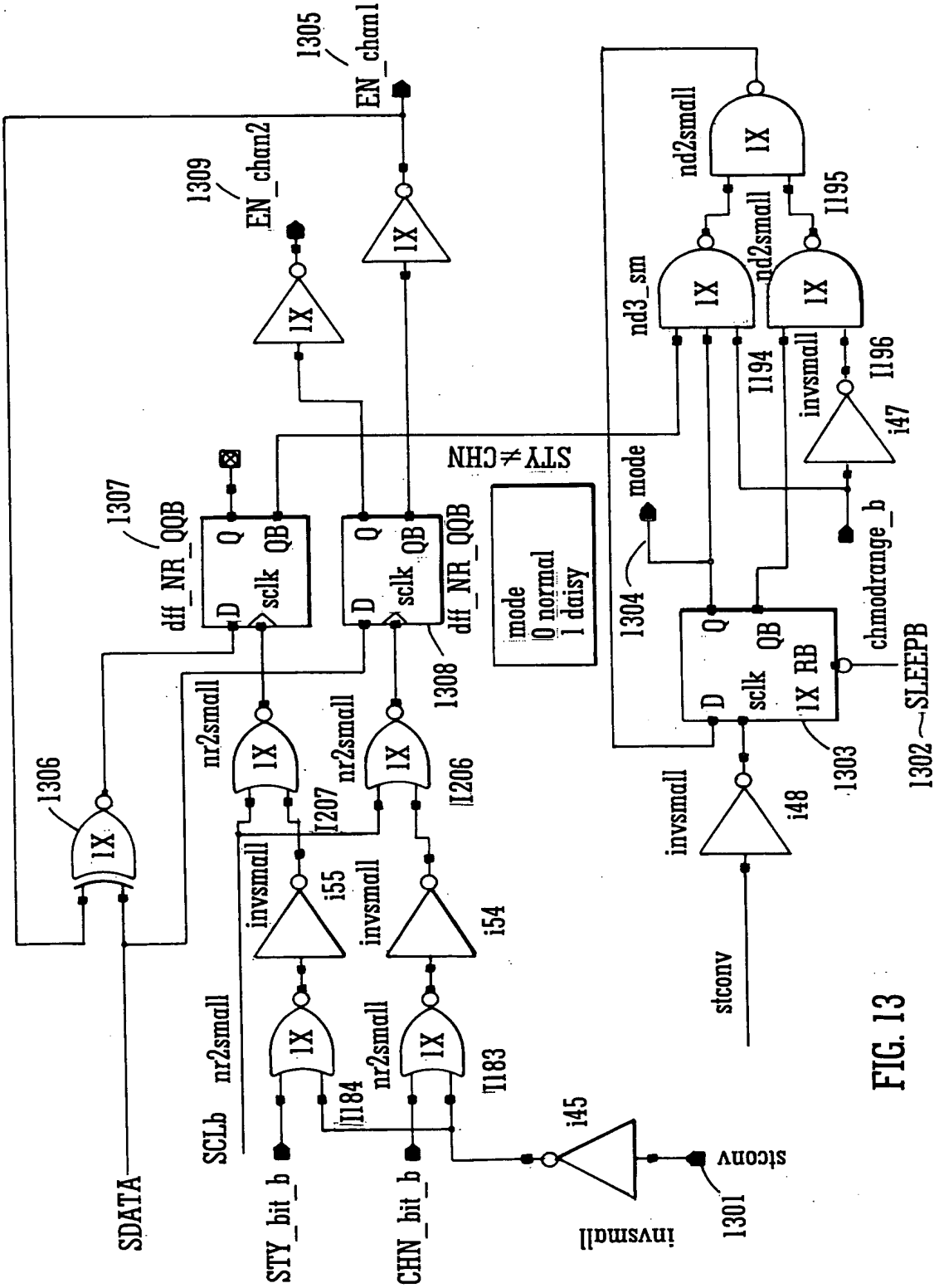

1305
EN_chan1
1309
EN_chan2
1X
1307
dff_NR_QQB
Q
QB
D
sclk
STY≠CHN
mode
0 normal
1 daisy
1308
1306
nr2small
I207
I206
invsmall
i55
i54
SCLb
SDATA
STY_bit_b
CHN_bit_b
I184
I183
i45
invsmall
sticonv
1301
stconv
i48
1303
1302
SLEEPB
1X RB
chmodrange_b
1304
mode
nd3_sm
I194
nd2small
I195
I196
i47

FIG. 13

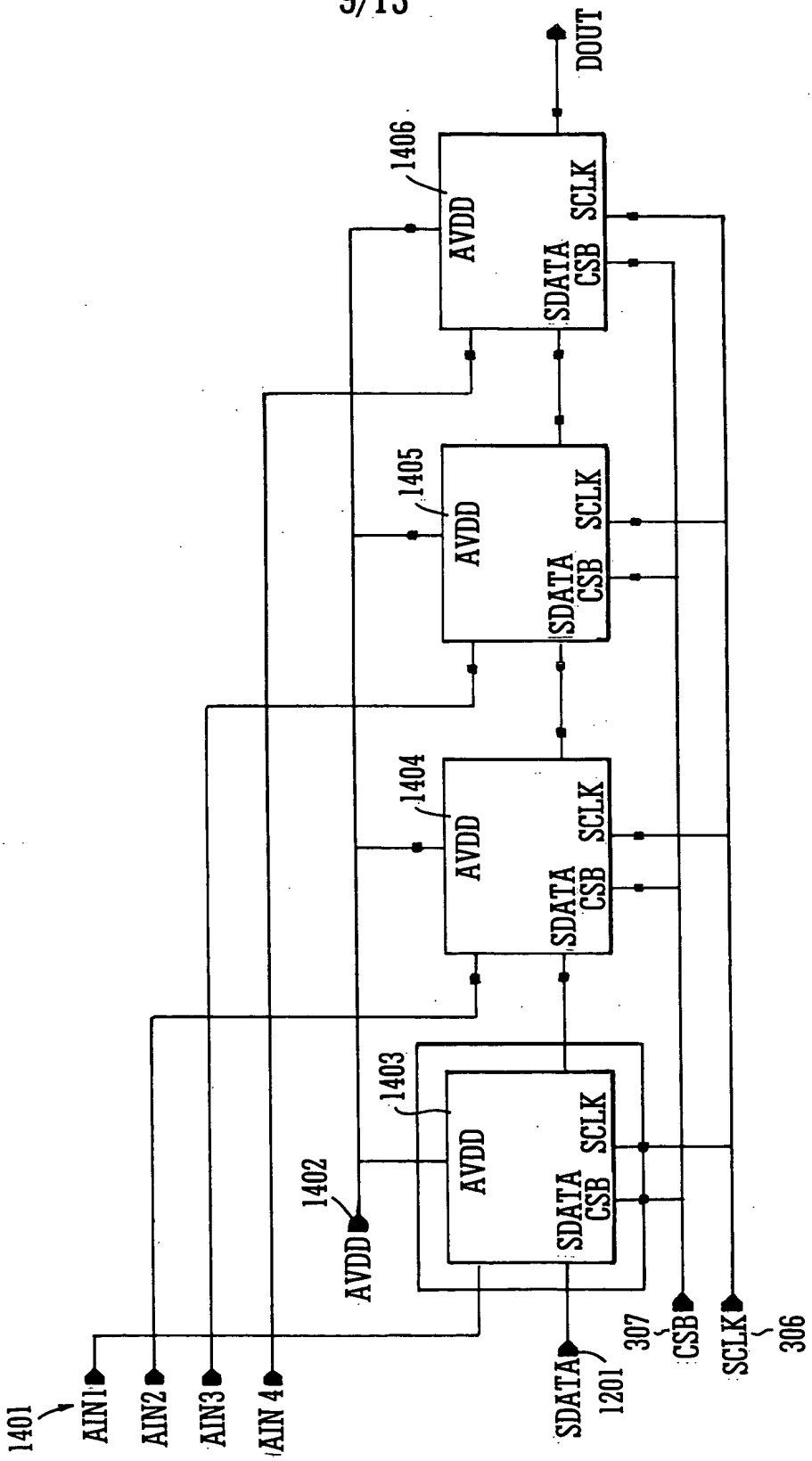

DOUT
1406
AVDD
SCLK
SDATA
CSB
1405
AVDD
SCLK
SDATA
CSB
1404
AVDD
SCLK
SDATA
CSB
1403
AVDD
SCLK
SDATA
CSB
1402
AVDD
1401
AIN1
AIN2
AIN3
AIN 4
SDATA
1201
307
CSB
SCLK
306

FIG. 14

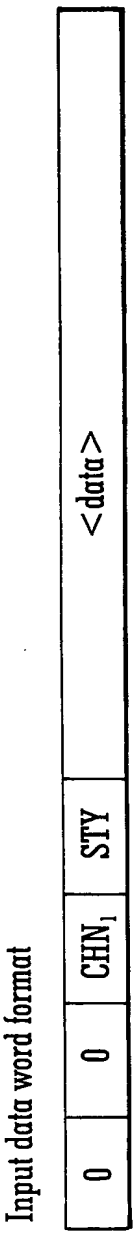

Input data word format
0
0
CHN1
STY
<data>

FIG. 15

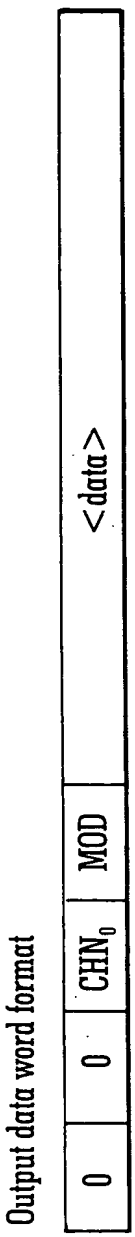

Output data word format
0
0
CHN0
MOD
<data>

FIG. 16

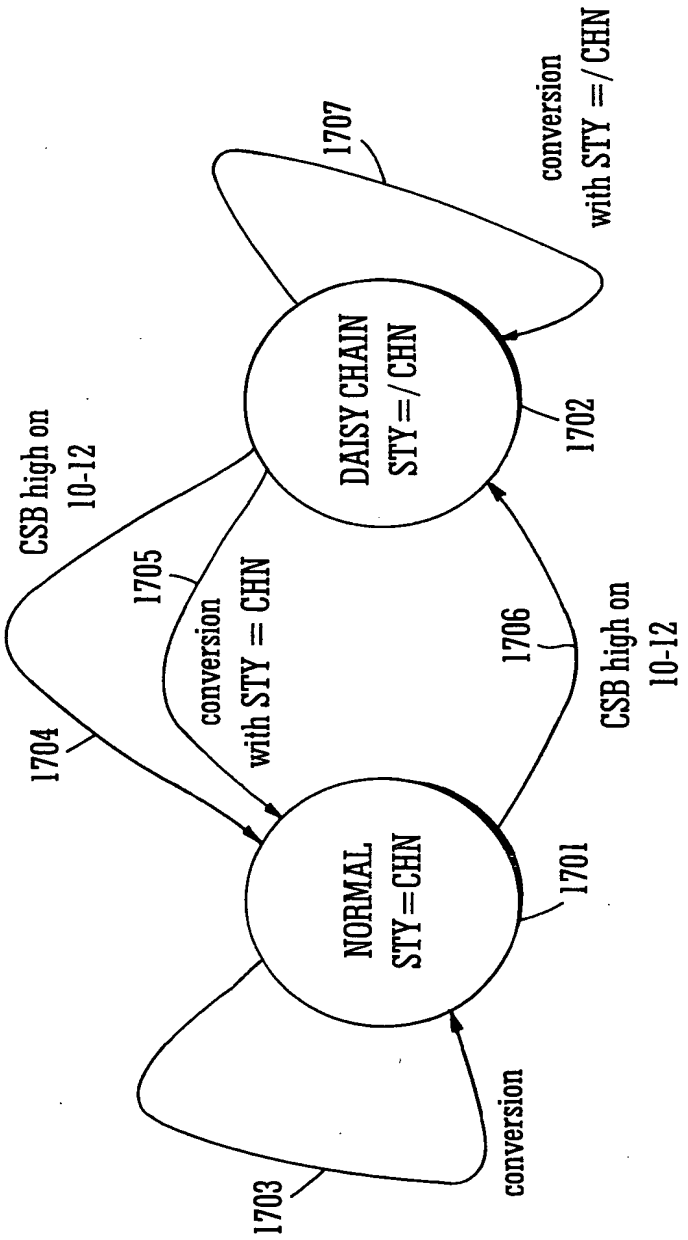

NORMAL
STY=CHN
1701
DAISY CHAIN
STY=/CHN
1702
conversion
1703
CSB high on
10-12
1704
conversion
with STY = CHN
1705
CSB high on
10-12
1706
1707
conversion
with STY =/CHN

FIG. 17

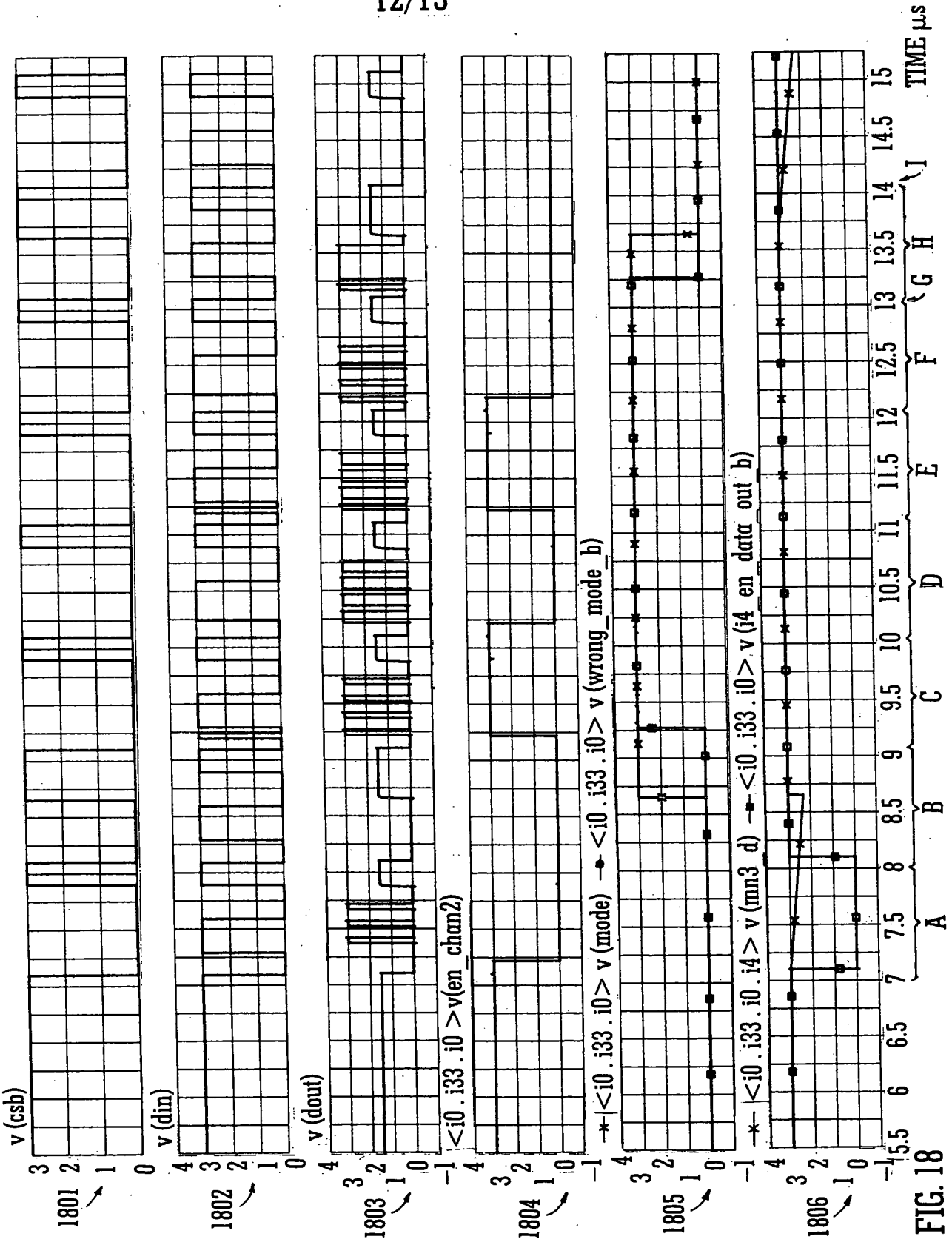

v (csb)
v (din)
v (dout)
<i0 .i33 .i0 >v(en_chan2)
*|<i0 .i33 .i0 > v (mode)
*|<i0 .i33 .i0 > v (wrong_mode_b)
*|<i0 .i33 .i0 .i4 > v (mn3 d)
*|<i0 .i33 .i0 > v (i4 en data out b)
1801
1802
1803
1804
1805
1806
TIME µs
A
B
C
D
E
F
G
H
I

FIG. 18

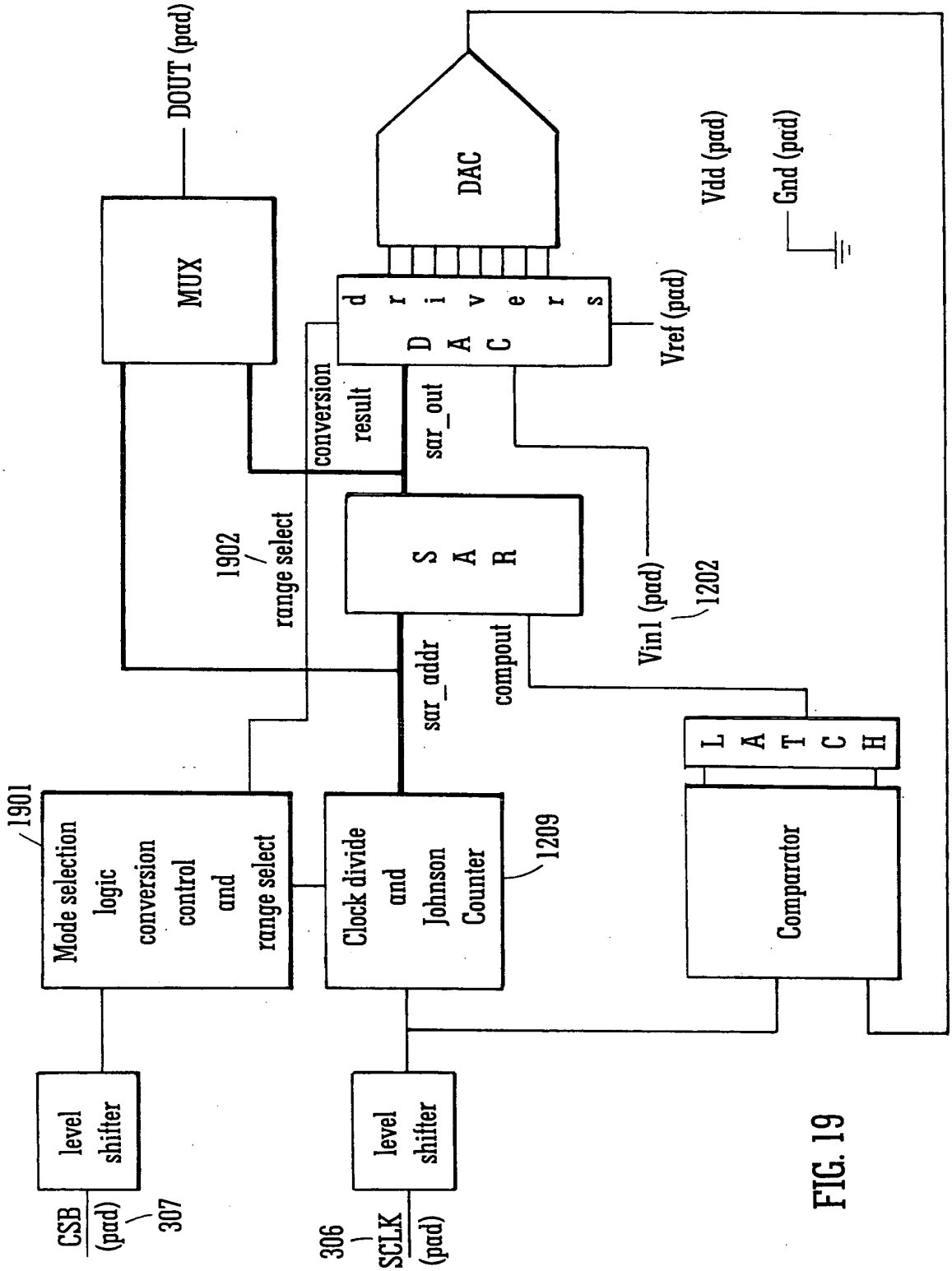

DOUT (pad)
MUX
DAC
Vdd (pad)
Gnd (pad)
d r i v e r s
D A C
Vref (pad)
conversion result
sar_out
1902
range select
S A R
Vin1 (pad)
1202
sar_addr
compout
L A T C H
1901
Mode selection logic conversion control and range select
Clock divide and Johnson Counter
1209
Comparator
level shifter
level shifter
CSB (pad)
307
306
SCLK (pad)

FIG. 19